WHAT IS CLAIMED IS:

1. A bus data interface that transmitting data on a PCI bus, comprising:

a high-bit transmitting buffer, to buffer a high-bit data;

a low-bit transmitting buffer, to buffer a low-bit data;

a multiplexer, coupled to the high-bit transmitting buffer and the low-bit transmitting buffer and receiving an internal bus clock, wherein the multiplexer alternatively outputs the high-bit transmitting data or the low-bit transmitting data to the PCI bus in response to a high potential level and a low potential level of the internal bus clock;

a strobe generator, to generate a data strobe signal in response to the internal bus clock when the bus data interface outputs data to the PCI bus; and

a data distributor, coupled to the PCI bus, for receiving the high-bit receiving data and the low-bit receiving data from the PCI bus in repines to the data strobe signal;

wherein the strobe generator uses either a bus grant signal pin or a bus request signal pin as an output pin to transmit the data strobe signal.

2. The bus data interface according to claim 1, wherein the bus data interface is applied to a bus master, and when the bus master is performing a data write operation, the bus request signal pin transmits a transmitting data strobe signal; and when the bus master performing a data read operation, the bus grant signal pin receives a receiving data strobe signal.

3. The bus data interface according to claim 1, wherein the bus data interface is applied to a bus host bridge that arbitrates a master control of the PCI bus according to the bus request signal and the bus grant signal; when the bus host bridge is outputting data to the PCI bus, the bus grant signal pin transmit a transmitting data strobe signal;

and when the bus host bridge is receiving data from the PCI bus, the bus request signal pin receive a receiving data strobe signal.

4. The bus data interface according to claim 1, further comprising a first-in-first-out memory coupled to the high-bit transmitting buffer and the low-bit transmitting buffer to receive a plurality of transmitting datainto the high-bit buffer and low-bit transmitting buffer respectively.

5. The bus data interface according to claim 1, further comprising:

a high-bit receiving buffer, coupled to the data distributor to buffer the high-bit receiving data; and

a low-bit receiving buffer, coupled to the data distributor to buffer the low-bit receiving data.

6. The bus data interface according to claim 1, wherein the data distributor further comprises:

a data buffer, coupled to the PCI bus to buffer the high-bit data and the low-bit receiving data;

a strobe signal buffer, to buffer the data strobe signal;

a first trigger latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to an output of the data buffer and the trigger terminal is coupled to the strobe signal buffer to latch either the high-bit or the low-bit receiving data according to the receiving data strobe signal;

a first negative enable latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to the output of the data buffer and the trigger terminal is coupled to the strobe signal buffer to latch whichever of the high-bit and low-bit receiving data that are not yet latched according

to the receiving data strobe signal;

a second trigger latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to the data output terminal of the first trigger latch, and the trigger terminal is coupled to the internal bus clock to output data of the data input terminal to the data output terminal synchronous to the internal bus clock; and

a second negative enable latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to the data output terminal of the first negative enable latch and the trigger terminal is coupled to the internal bus clock to output data of the data input terminal to the data output terminal synchronous to the internal bus clock.

7. The bus data interface according to claim 1, wherein the data distributor further comprises:

a data buffer, coupled to the PCI bus to receive and output the high-bit and low-bit receiving data;

a strobe signal buffer, to receive and output the receiving data strobe signal;

a first trigger latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to an output of the data buffer and the trigger terminal is coupled to the strobe signal buffer to latch either the high-bit or low-bit receiving data according to the receiving data strobe signal;

a first negative enable latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to the output of the data buffer and the trigger terminal is coupled to the strobe signal buffer to latch whichever of the high-bit and low-bit receiving data are not yet latched according to the

receiving data strobe signal;

a second trigger latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled the data output terminal of the first negative enable latch and the trigger terminal is coupled to the internal bus clock to output data of the data input terminal to the data output terminal synchronous to the internal bus clock; and

a second negative enable latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled the data output terminal of the first trigger latch and the trigger terminal is coupled to the internal bus clock to output data of the data input terminal to the data output terminal synchronous to the internal bus clock

8. A bus structure to transmit data on a PCI bus, wherein the PCI bus comprises a bus grant signal and a bus request signal, the bus structure comprising:

a transmission compatible apparatus, coupled to the PCI bus, further comprising:

a high-bit transmitting buffer, to receive and temporarily store a high-bit transmitting data;

a low-bit transmitting buffer, to receive and temporarily store a low-bit transmitting data;

a multiplexer, coupled to the high-bit and low-bit transmitting buffers to receive a first internal bus clock signal, wherein the multiplexer alternatively outputs the high-bit transmitting data or the low-bit transmitting data to the PCI bus in response to a high potential level and a low potential level of the internal bus clock; and

astrobe generator, for generating a data strobe signal according to the first internal bus clock signal when the transmission compatible apparatus is coupled to

the PCI bus;

a reception compatible apparatus, coupled to the PCI bus and comprising:

a data distributor, coupled to the PCI bus and receiving data from the PCI bus and outputting a high-bit receiving data and a low-bit receiving data in response to the data strobe signal.

9. The bus structure according to claim 8, wherein the transmission compatible apparatus is applied to a bus master, and the reception compatible apparatus is applied to a bus host bridge, wherein the bus host bridge arbitrates a master control of the PCI bus according to the bus request signal and the bus grant signal, and when the bus master is outputting data to the PCI bus, the bus request signal pin transmits thedata strobe signal.

10. The bus structure according to claim 8, wherein the reception compatible apparatus is applied to a bus master and the transmission compatible apparatus is applied to a bus host bridge, wherein the bus host bridge arbitrates a master control of the PCI bus according to the bus request signal and the bus grant signal, and when the bus master is outputting data to the PCI bus, the bus grant signal pin receives the data strobe signal.

11. The bus structure according to claim 8, wherein the transmission compatible apparatus further comprises a first-in-first-out memory coupled to the high-bit transmitting buffer and the low-bit transmitting buffer to sequentially transmit the high-bit data and low-bit transmitting data to the high-bit and low-bit transmitting buffers, respectively.

12. The bus structure according to claim 8, wherein the reception compatible apparatus further comprises:

a high-bit receiving buffer, coupled to the data distributor to buffer the high-bit receiving data; and

a low-bit receiving buffer, coupled to the data distributor to buffer the low-bit receiving data

13. The bus structure according to claim 8, wherein the data distributor further comprises:

a data buffer, coupled to the PCI bus to receive and output the high-bit and low-bit receiving data;

a strobe signal buffer, to receive and output the data strobe signal;

a first trigger latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to an output of the data buffer and the trigger terminal is coupled to the strobe signal buffer to latch either the high-bit or the low-bit receiving data according to the data strobe signal;

a first negative enable latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to the output of the data buffer and the trigger terminal is coupled to the strobe signal buffer to latch whichever of the high-bit and low-bit receiving data are not yet latched according to the data strobe signal;

a second trigger latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled the data output terminal of the first trigger latch and trigger terminal is coupled to a second internal bus clock to output data of the data input terminal to the data output terminal synchronous to the internal bus clock; and

a second negative enable latch, comprising a data input terminal, a trigger

terminal and a data output terminal, wherein the data input terminal is coupled the data output terminal of the first negative enable latch and the trigger terminal is coupled to the second internal bus clock to output data of the data input terminal to the data output terminal synchronous to the second internal bus clock.

14. The bus data interface according to claim 8, wherein the data distributor further comprises:

a data buffer, coupled to the PCI bus to receive and output the high-bit and low-bit receiving data;

a strobe signal buffer, to receive and output the data strobe signal;

a first trigger latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to an output of the data buffer, and the trigger terminal is coupled to the strobe signal buffer to latch either the high-bit or the low-bit receiving data according to the data strobe signal;

a first negative enable latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled to the output of the data buffer, and the trigger terminal is coupled to the strobe signal buffer to latch whichever of the high-bit and low-bit receiving data are not yet latched according to the data strobe signal;

a second trigger latch, comprising a data input terminal, a trigger terminal and a data output terminal, wherein the data input terminal is coupled the data output terminal of the first negative enable latch, and trigger terminal is coupled to a second internal bus clock to output data of the data input terminal to the data output terminal synchronous to the second internal bus clock; and

a second negative enable latch, comprising a data input terminal, a trigger

terminal and a data output terminal, wherein the data input terminal is coupled the data output terminal of the first trigger latch, and trigger terminal is coupled to the second internal bus clock to output data of the data input terminal to the data output terminal synchronous to the second internal bus clock.

15. A method for transmitting data on a PCI bus , in a computer comprises a plurality of masters and a host bridge coupled to the PCI bus, said PCI bus having a plurality of bus request signals and a plurality of bus grant signals, the method comprising:

detecting whether individual master supports a dual transmission mode while starting up the computer; and

asserting the corresponding bus request signal of individual master supporting the dual transmission mode.

16. The method according to claim 15, further comprising:

judging whether the corresponding master corresponding to one of the bus request signals supports the dual transmission mode according to said corresponding bus request signal;

outputting a dual mode ID when the dual transmission mode is required; and

activating the dual transmission mode in response to the dual mode ID.

17. The method according to claim 15, wherein the detecting step comprises:

comparing a vendor's ID and a device ID of the individual master with a status list to determine whether the individual master supports the dual transmission mode.

18. The method according to claim 15, further comprising:

programming a host bridge in response to the masters supporting the dual transmission mode.

19. The method according to claim 16,, wherein the dual mode ID is determined in response to two least significant bits of an address signal.

20. The method according to claim 19, wherein said two least significant bits of the address signal are configured as 2.

21. The method according to claim 18, further comprising:

granting the PCI bus to one of the masters supporting the dual transmission mode;

asserting a dual mode ID by said master supporting the dual transmission mode; and

performing a memory access at a dual speed while accessing in a range of a memory space supporting the dual transmission mode.

22. The method according to claim 21, further comprising:

performing a memory access at a normal speed while not accessing in the range of the memory space supporting the dual transmission mode.